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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,004	FORBES ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-39,59-61,71-85,98 and 99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *83-85* is/are allowed.

6)☒ Claim(s) *36-39,59-61,71-82,98 and 99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The examiner has considered the items listed on the Information Disclosure Statement filed 12/08/2003. Please find enclosed a signed copy of Form PTO-1449.

Response to Arguments

1. Applicant's arguments filed 12/08/2003 have been fully considered but they are not persuasive.

With regard to the traverse of Rejections of Claims under § 102:

Applicant's traverse appears to be based on claim 37 reciting that the stoichiometric parameter x "is approximately between 0.5 and 1.0, and this does not include 0.5". However, the adverb "approximately" implies the range from 0.5 to 1.0 to have a variance with respect to both end points, and hence Applicant's allegation is incorrect and claim 37 is not in condition for allowance.

With regard to the traverse of Rejections of Claims under § 103:

Applicant's traverse of the rejection of claim 36 Applicant alleges that a *prima facie* case of obviousness is not established when, as in this case the claimed range and the prior art range are infinitesimally removed from overlapping. However, the cited case law, In re Peterson, 65 USPQ2d 1379 (Fed. Cir. 2003) precisely addresses the issue at hand in explaining the affirmation of the rejections. To quote:

"*Peterson thus contends that the examiner and the Board failed to appreciate the criticality of and the unexpected results achieved by the claimed combination of about 1-3% rhenium with,*

among other elements, about 14% chromium. Peterson further argues that Wukusick and Bieber teach away from the claimed invention by warning that high chromium contents can adversely affect alloy strength. The PTO responds that the Board correctly found that the claimed composition would have been obvious based on any one of the three grounds of rejection because Shah, Wukusick, and Bieber all disclose ranges of elements that overlap the claimed ranges. The PTO argues that the Board properly interpreted the phrase "about 14 percent chromium" to include Wukusick's 12% chromium because Example I in Peterson's application discloses a superalloy containing 12.03% chromium". The Board continues:

"*We have also held that a prima facie case of obviousness exists when the claimed range and the prior art range do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. Titanium Metals Corp. v. Banner, 778 F.2d 775, 783, 227 USPQ 773, 779 (Fed. Cir. 1985)*" and it is in this regard that the case law as cited is absolutely pertinent to the issue at hand. In fact, the ranges cannot possibly be closer, because their difference is infinitesimal, i.e., any further approach between said ranges, no matter how small, would cause overlap. It is clear to anyone of ordinary skills in the art that such infinitesimal change does not impart any substantial change in the transistor.

Parenthetically, no reliance is made on any theory in the sense of Applicant, which is implied to be an unsubstantiated "theory" (there are other kinds that are in fact quite substantiated and Applicant would be well-advised to keep in mind the theoretical component of all experimentation, "theory", as opposed to "model" being reserved for a mathematical description with substantial experimental confirmation), in that a discontinuity at x=0.5 of any kind in the functioning of the device would be an

unexpected result for anyone of ordinary skills in the art. Applicant's burden comprises to show unexpected results and Applicant has not met said burden.

Therefore, the examiner sees neither reason nor possibility to withdraw the rejection of claim 36.

With regard to the traverse of the rejections of claims 59-61 under § 103:

Again Applicant's argument of traverse appears to be that the Office Action "is relying on a scientific theory here", by stating that "even in ultra-amorphous state nanocrystals, i.e., crystals at the scale of the interatomic distance, exist". But, once again, no "theory" has been either cited or advanced, the above statement merely having been added to underscore the lack of any true limitation implied by claim 61. Said statement is not theory but fact, because a nanometer is at most about 2 to 3 interatomic distances (see any data collection such as "Semiconductors – Basic Data, 2nd Revised Edition, Editor: Otfried Madelung, Springer Verlag, Berlin, Heidelberg and New York 1996, pages 49-53) which logically implies that any lack of periodicity cannot be established on the scale of simple bonds. Moreover, with regard to the core of the argument used in the rejection of claim 61, Halvis et al teach the manufacture of the silicon carbide by adding carbon to polysilicon (col. 3, l. 31) and thus necessarily producing silicon carbide that is polycrystalline, while polysilicon is also the ground material for the invention by Chiang. Applicant has not presented arguments in traverse of this reason based on the teaching by Halvis et al to produce silicon carbide by adding carbon to polysilicon. Therefore, the rejection of claims 59-61 stand.

With regard to the traverse of the rejections of claims 37 and 99 under 35 USC § 103:

Applicant presented no arguments of traverse other than those presented in traverse of the rejection of claim 36, and therefore the rejection is made to stand with reference to the above discussion of the arguments of traverse of the rejection of claim 36.

With regard to the traverse of the rejections of claims 62-67 under 35 USC § 103:

A statement of traverse is noted. However, claims 62-67 have been cancelled, and therefore said traverse is found moot.

With regard to the traverse of the rejections of claims 71-73 under 35 USC § 103:

Applicant's traverse (page 12) is based on the allegation that motivation is absent because "there is no evidence that Nakamura detects light that traverses a floating gate". However, the motivation presented in the Office Action was based on the teaching by Halvis et al in wholly analogous art (photo detectors) that the gate may be improved by making it transparent by adding up to 50% carbon, thus increasing the efficiency of detection, while the floating gate in Nakamura covers the surface through which light enters the upper surface of the p-substrate (Nakamura et al, Figure 1), and hence motivation is evident: through the improvement for the gate as taught by Halvis et al the gate in Nakamura et al no longer optically covers the sensitive p-substrate in the photo detector and hence light detection is made more efficient. The rejection is thus made to stand.

With regard to the traverse of the rejections of claims 74 and 76 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 71-73. The rejections therefore stand.

With regard to the traverse of the rejection of claim 75 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 71-73. The rejection therefore stands.

With regard to the traverse of the rejections of claim 77 and 79 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 71-73. Therefore, the rejections stand.

With regard to the traverse of the rejection of claim 78 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 75.

With regard to the traverse of the rejections of claims 80-82 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 71-73. Therefore, the rejections stand.

With regard to the traverse of the rejections of claims 36 and 98 under 35 USC § 103:

Applicant does not provide arguments of traverse independent of those already presented and discussed in connexion with claims 71-73. Therefore, the rejections stand.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. ***Claim 37*** is rejected under 35 U.S.C. 102(e) as being anticipated by Weitzel et al (5,661,312). Weitzel et al teach a source region 21 (cf. col. 2, l. 2), a drain region 11 (cf. col. 1, l. 42-44 and col. 2, l. 4-5), a channel region 14 (cf. col. 1, 50) between said source region and said drain region, and a gate 18 (cf. col. 1, l. 57-58) separated from said channel region by an insulator 17 (cf. col. 1, 52), and furthermore are inherent in the device by Weitzel et al, because all of the above limitations are inherent in a MOSFET as disclosed by Weitzel et al in their abstract and claimed (claim1 for instance). Furthermore, the gate as claimed in by Weitzel et al in their claim 2 dependent upon their claim 1, is in one embodiment made of a silicon carbide compound $Si_{1-x}C_x$ with x=0.5, namely: silicon carbide (SiC). Therefore, Weitzel et al

teach the gate formed of a silicon carbide compound $Si_{1-x}C_x$ with x selected at a predetermined value approximately between 0.5 and 1.0. The value for x of the prior art is thus seen to be within the claimed range defined in claim 37. The purpose as claimed, i.e., "to establish a desired value of a barrier energy between the gate and the insulator" is irrelevant for the present device claim, for which only the final structure matters.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claim 36 and 38-39*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (4,598,305) in view of Halvis et al (5,369,040). Chiang et al teach (cf. Fig. 1) a transistor comprising a source region, a drain region, a channel region between the source and drain regions (regions 26, 28 are the source/drain regions, and 16 is a channel region) (cf. col. 3, l. 32-66); and a (polysilicon) gate 22 separated from the channel region by an insulator 20 (cf. col. 3, l. 32-66). The gate 22 according to Chiang is of silicon (cf. col. 3, l. 32-66). Although Chiang et al do not necessarily teach the gate material to be $Si_{1-x}C_x$ with x between 0.5 and 1.0, it would have been obvious to replace the poly-silicon gate material with $Si_{1-x}C_x$ with x being infinitesimally close to the range x greater than 0.5 in view of Halvis et al, who teach in the art of MOS photo-

detectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon to the poly-silicon, thus creating a polycrystalline silicon carbide compound gate, thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). Applicant's disclosure does not explain why it is critical to the invention to make x infinitesimally greater than 0.5 instead of infinitesimally less than 0.5: the "Summary of the Invention" rather allows for the range $0 < x < 1$ (see pages 3-5), while other claims in the same invention cover rather complementary ranges, such as $0.1 < x < 0.5$. Furthermore, according to Applicant the value of x in one embodiment is selected to establish a desired value for the barrier energy between the gate and the underlying insulator; however, the energy gap of $Si_{1-x}C_x$, and hence said barrier energy is a continuous function of the stoichiometric parameter x. Therefore, said barrier energy has substantially the same value for x=0.5 and for x infinitesimally greater than 0.5. The burden is to Applicant to show otherwise, i.e., to show said infinitesimal difference in x makes a critical difference in the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 38: The barrier energy between the gate material in the device as essentially taught by Chiang et al and Halvis et al is the barrier energy between silicon dioxide (cf. col. 3, l. 56-58 in Chiang et al) and $Si_{1-x}C_x$ with x infinitesimally close to but

less than 0.5; said barrier energy is therefore infinitesimally close to a boundary in the claimed range, namely 2.8 eV. Applicant neither discloses nor explains in the Specification why said infinitesimal difference is critical to the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 39: the insulator in the invention as essentially taught by Chiang et al and Halvis et al is formed of silicon dioxide (cf. col. 3, l. 56-58 in Chiang et al).

5. ***Claims 59-61*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (4,598,305) and Halvis et al (5,369,040). Chiang et al teach (cf. Fig. 1) a transistor comprising a source region and a drain region (regions 26 and 28) formed in a substrate 12/14/22, a channel region 16 in the substrate between the source and drain regions (cf. col. 3, l. 32-66); and a (polysilicon) gate 22 separated from the channel region by an insulator 20 (cf. col. 3, l. 32-66). The gate 22 according to Chiang is of silicon (cf. col. 3, l. 32-66). Although Chiang et al do not necessarily teach the gate material to be $Si_{1-x}C_x$ with x between approximately 0.5 and 1.0, it would have been obvious to replace the poly-silicon gate material with $Si_{1-x}C_x$ with x up to 0.5 in view of Halvis et al, who teach in the art of MOS photo-detectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon

to the poly-silicon, thus creating a polycrystalline silicon carbide compound gate, thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). Applicant's disclosure does not explain why it is critical to the invention to make x infinitesimally greater than 0.5 thus fulfilling the limitation in the claim, instead of infinitesimally less than 0.5 as taught by Halvis et al: the "Summary of the Invention" rather allows for the range $0 < x < 1$ (see pages 3-5), while other claims in the same invention cover rather complementary ranges, such as $0.1 < x < 0.5$. Furthermore, according to Applicant the value of x in one embodiment is selected to establish a desired value for the barrier energy between the gate and the underlying insulator; however, the energy gap of $Si_{1-x}C_x$, and hence said barrier energy is a continuous function of the stoichiometric parameter x (a polynomial). Therefore, said barrier energy has substantially the same value for x=0.5 and for x infinitesimally greater than 0.5. The burden is to Applicant to show otherwise, i.e., to show said infinitesimal difference in x makes a critical difference in the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). Because the device by Chiang et al detects light that traverses the gate material there is ample motivation to include the teaching by Halvis et al in this respect in the device by Chiang et al. Combination of said teaching and said device is straightforward by adding methane gas during poly-silicon growth or using ion implantation as recommended by

Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

On claim 60: the substrate in the device by Chiang et al comprises a p-type silicon substrate 14 (cf. col. 3, l. 46-55); the source region comprises an n+ type source region formed in the substrate and the drain region comprises an n+ type drain region in the substrate (regions 26 and 28, respectively) (cf. col. 3, l. 60-66); and the insulator 20 comprises a layer of silicon dioxide (cf. col. 3, l. 56-58).

On claim 61: the insulator according to Chiang et al is made of silicon dioxide, because said insulator is made by oxidizing part of the polysilicon layer 22 (cf. col. 3, l. 56-58); furthermore, the methods of making the $Si_{1-x}C_x$ gate as described by Halvis et al produce $Si_{1-x}C_x$ from polycrystalline silicon thus creating crystalline silicon carbide at least on the molecular scale, i.e., nano-crystalline silicon carbide. Finally, there is no difference in the meaning of the verbiage "nanocrystalline" and the meaning of the verbiage "amorphous" because even in an ultra-amorphous state nanocrystals, i.e., crystals at the scale of the interatomic distance, exist. Therefore, the list of crystalline forms that constitutes the essence of this claim is not a true limitation.

6. ***Claims 37 and 99*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al (4,598,305) in view of Halvis et al (5,369,040). Chiang et al teach (cf. Fig. 1) a transistor comprising a source region, a drain region, a channel region between the source and drain regions (regions 26, 28 are the source/drain regions, and 16 is a channel region) (cf. col. 3, l. 32-66); and a (polysilicon) gate 22 separated from

the channel region by an insulator 20 (cf. col. 3, l. 32-66). The gate 22 according to Chiang is of silicon (cf. col. 3, l. 32-66). Although Chiang et al do not necessarily teach the gate material to be $Si_{1-x}C_x$ with x between approximately 0.5 and 1.0, it would have been obvious to replace the poly-silicon gate material with $Si_{1-x}C_x$ with x falling in the range between approximately 0.5 and 1.0 in view of Halvis et al, who teach in the art of MOS photo-detectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon to the poly-silicon, thus creating a polycrystalline silicon carbide compound gate, thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). Because the device by Chiang et al detects light that traverses the gate material there is ample motivation to include the teaching by Halvis et al in this respect in the device by Chiang et al. Combination of said teaching and said device is straightforward by adding methane gas during poly-silicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

On claim 99: the insulator according to Chiang et al is made of silicon dioxide, because said insulator is made by oxidizing part of the polysilicon layer 22 (cf. col. 3, l. 56-58); furthermore, the methods of making the $Si_{1-x}C_x$ gate as described by Halvis et al produce $Si_{1-x}C_x$ from polycrystalline silicon thus creating crystalline silicon carbide at least on the molecular scale, i.e., nano-crystalline silicon carbide. Finally, there is no difference in the meaning of the verbiage "nanocrystalline" and the meaning of the verbiage "amorphous" because even in an ultra-amorphous state nanocrystals, i.e.,

crystals at the scale of the interatomic distance, exist. Therefore, the list of crystalline forms that constitutes the essence of this claim is not a true limitation.

7. ***Claims 71-73*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (ISSN #: 0018-9383) in view of Halvis et al (5,369,040). Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The floating gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

Nakamura et al do not necessarily teach the further limitation that the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$ with x selected between 0.5 and 1.0. However, it would have been obvious to replace the floating gate material with $Si_{1-x}C_x$ with x between 0.1 and 0.5 in view of Halvis et al, who teach in the art of MOS

photodetectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon, i.e., only infinitesimally less than x>0.5, to the silicon, thus creating a polycrystalline silicon carbide compound gate (therefore, the added further limitation defined by *claim 73* is met), thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). The prior art range thus only infinitesimally fails to overlap with the range as claimed. Applicant's disclosure does not explain why it is critical to the invention to make x infinitesimally greater than 0.5 thus fulfilling the limitation in the claim, instead of infinitesimally less than 0.5 as taught by Halvis et al: the "Summary of the Invention" rather allows for the range $0 < x < 1$ (see pages 3-5), while other claims in the same invention cover rather complementary ranges, such as $0.1 < x < 0.5$. Furthermore, according to Applicant the value of x in one embodiment is selected to establish a desired value for the barrier energy between the gate and the underlying insulator; however, the energy gap of $Si_{1-x}C_x$, and hence said barrier energy is a continuous function of the stoichiometric parameter x (a polynomial). Therefore, said barrier energy has substantially the same value for x infinitesimally less than 0.5 and for x infinitesimally greater than 0.5. The burden is to Applicant to show otherwise, i.e., to show said infinitesimal difference in x makes a critical difference in the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). Because the device by Chiang et al detects

light that traverses the gate material there is ample motivation to include the teaching by Halvis et al in this respect in the device by Chiang et al. Combination of said teaching and said device is straightforward by adding methane gas during poly-silicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

Because the device by Nakamura et al detects light that traverses the floating gate (FG) material (because the active region is located between the n+ source and drain regions) (see Figure 1) there is ample motivation to include the teaching by Halvis et al in this respect in the device by Nakamura et al. Combination of said teaching and said device is straightforward by adding methane gas during polysilicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

On claim 72: Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The floating gate is made of polysilicon (double-poly

process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

8. ***Claims 74 and 76*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (ISSN #: 0018-9383) in view of Halvis et al (5,369,040). Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The floating gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

Nakamura et al do not necessarily teach the further limitation that the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$ with x selected between 0.1 and 0.5. However, it would have been obvious to replace the floating gate material with

$Si_{1-x}C_x$ with x between 0.1 and 0.5 in view of Halvis et al, who teach in the art of MOS photodetectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon, i.e., less than x=0.5, to the silicon, thus creating a polycrystalline silicon carbide compound gate (therefore, the added further limitation defined by *claim 76* is met), thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). The range $x<0.5$ completely includes the range by Applicant while the preferred value of x being approximately 10% still is in the range of Applicant. Because the device by Nakamura et al detects light that traverses the floating gate (FG) material (because the active region is located between the n+ source and drain regions) (see Figure 1) there is ample motivation to include the teaching by Halvis et al in this respect in the device by Nakamura et al. Combination of said teaching and said device is straightforward by adding methane gas during polysilicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

9. ***Claim 75*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Halvis et al as applied to claim 74 above, and further in view of Chiang et al (4,598). As detailed above, independent claim 74 is unpatentable over Nakamura et al in view of Halvis et al. Furthermore, the substrate in the device by Nakamura et al comprises a p-type silicon substrate p (cf. Figure 1 and page 1694, "Image Sensor Architecture", first paragraph, referring to double-poly CMOS process; see Wolf pages 311-312 for definition of double-poly CMOS process); the source and

drain region comprise n+ type source and drain regions n+ (cf. col. 3, l. 32-66); and the insulator comprises a layer of silicon dioxide (cf. col. 3, l. 32-66) as it is grown by oxidizing the silicon layer 16. Although neither Nakamura et al nor Halvis et al necessarily teach the insulator to be of silicon dioxide, silicon dioxide is a preferred selection for the gate insulation layer in any MOSFET because of its ease of making and has been used by for instance Chiang et al in the analogous art of MOS photodetectors (cf. Figure 1, col. 3, l. 56-58), in which one of the requirements involves the relative transparency of the gate insulator material to light.

Motivation to include the teaching by Chiang et al in the device as essentially taught by Nakamura et al and Halvis et al stems from said relative ease of making according to the method delineated by Chiang et al (cf. col. 3, l. 56-58) and from said relative transparency to light. Combination of said teaching with said device merely involves a standard step in the double-poly process followed by Nakamura et al through which the entire device can be made starting from silicon.

10. ***Claims 77 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (ISSN #: 0018-9383) in view of Halvis et al (5,369,040). Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said

source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The floating gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

Nakamura et al do not necessarily teach the further limitation that the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$ with x selected to be less than 0.5. However, it would have been obvious to replace the floating gate material with $Si_{1-x}C_x$ with x less than 0.5 in view of Halvis et al, who teach in the art of MOS photodetectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon, i.e., less than x=0.5, to the silicon, thus creating a polycrystalline silicon carbide compound gate (therefore, the added further limitation defined by *claim 79* is met), thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). Because the device by Nakamura et al detects light that traverses the floating gate (FG) material (because the active region is located between the n+ source and drain regions) (see Figure 1) there is ample motivation to include the teaching by Halvis et al in this respect in the device by Nakamura et al. Combination of said teaching and said device is straightforward by adding methane gas during polysilicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l.

44-51). Success in implementing the combination can therefore be reasonably expected.

11. ***Claim 75*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Halvis et al as applied to claim 74 above, and further in view of Chiang et al (4,598). As detailed above, independent claim 74 is unpatentable over Nakamura et al in view of Halvis et al. Furthermore, the substrate in the device by Nakamura et al comprises a p-type silicon substrate p (cf. Figure 1 and page 1694, "Image Sensor Architecture", first paragraph, referring to double-poly CMOS process; see Wolf pages 311-312 for definition of double-poly CMOS process); the source and drain region comprise n+ type source and drain regions n+ (cf. col. 3, l. 32-66); and the insulator comprises a layer of silicon dioxide (cf. col. 3, l. 32-66) as it is grown by oxidizing the silicon layer 16. Although neither Nakamura et al nor Halvis et al necessarily teach the insulator to be of silicon dioxide, silicon dioxide is a preferred selection for the gate insulation layer in any MOSFET because of its ease of making and has been used by for instance Chiang et al in the analogous art of MOS photodetectors (cf. Figure 1, col. 3, l. 56-58), in which one of the requirements involves the relative transparency of the gate insulator material to light.

Motivation to include the teaching by Chiang et al in the device as essentially taught by Nakamura et al and Halvis et al stems from said relative ease of making according to the method delineated by Chiang et al (cf. col. 3, l. 56-58) and from said relative transparency to light. Combination of said teaching with said device merely

involves a standard step in the double-poly process followed by Nakamura et al through which the entire device can be made starting from silicon.

12. ***Claim 78*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al and Halvis et al as applied to claim 77 above, and further in view of Chiang et al (4,598). As detailed above, independent claim 77 is unpatentable over Nakamura et al in view of Halvis et al. Furthermore, the substrate in the device by Nakamura et al comprises a p-type silicon substrate p (cf. Figure 1 and page 1694, "Image Sensor Architecture", first paragraph, referring to double-poly CMOS process; see Wolf pages 311-312 for definition of double-poly CMOS process); the source and drain region comprise n+ type source and drain regions n+ (cf. col. 3, l. 32-66); and the insulator comprises a layer of silicon dioxide (cf. col. 3, l. 32-66) as it is grown by oxidizing the silicon layer 16. Although neither Nakamura et al nor Halvis et al necessarily teach the insulator to be of silicon dioxide, silicon dioxide is a preferred selection for the gate insulation layer in any MOSFET because of its ease of making and has been used by for instance Chiang et al in the analogous art of MOS photodetectors (cf. Figure 1, col. 3, l. 56-58), in which one of the requirements involves the relative transparency of the gate insulator material to light.

Motivation to include the teaching by Chiang et al in the device as essentially taught by Nakamura et al and Halvis et al stems from said relative ease of making according to the method delineated by Chiang et al (cf. col. 3, l. 56-58) and from said relative transparency to light. Combination of said teaching with said device merely

involves a standard step in the double-poly process followed by Nakamura et al through which the entire device can be made starting from silicon.

13. ***Claims 80-82*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al ((ISSN #: 0018-9383) in view of Halvis et al (5,369,040). Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The floating gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

Nakamura et al do not necessarily teach the further limitation that the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$ with x selected to be between 0.5 and 0.75. However, it would have been obvious to replace the floating gate material with $Si_{1-x}C_x$ with x only infinitesimally less than 0.5 in view of Halvis et al, who

teach in the art of MOS photodetectors (cf. title and abstract), hence analogous art, that the gate can be made more transparent by adding up to 50% carbon, i.e., up to infinitesimally less than x=0.5, to the silicon, thus creating a polycrystalline silicon carbide compound gate (therefore, the added further limitation defined by *claim 82* is met), thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43).

The prior art range thus only infinitesimally fails to overlap with the range as claimed. Applicant's disclosure does not explain why it is critical to the invention to make x infinitesimally greater than 0.5 thus fulfilling the limitation in the claim, instead of infinitesimally less than 0.5 as taught by Halvis et al: the "Summary of the Invention" rather allows for the range $0 < x < 1$ (see pages 3-5), while other claims in the same invention cover rather complementary ranges, such as $0.1 < x < 0.5$. Furthermore, according to Applicant the value of x in one embodiment is selected to establish a desired value for the barrier energy between the gate and the underlying insulator; however, the energy gap of $Si_{1-x}C_x$, and hence said barrier energy is a continuous function of the stoichiometric parameter x (a polynomial). Therefore, said barrier energy has substantially the same value for x infinitesimally less than 0.5 and for x infinitesimally greater than 0.5. The burden is to Applicant to show otherwise, i.e., to show said infinitesimal difference in x makes a critical difference in the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson,

65 USPQ2d 1379 (CA FC 2003). Because the device by Chiang et al detects light that traverses the gate material there is ample motivation to include the teaching by Halvis et al in this respect in the device by Chiang et al. Combination of said teaching and said device is straightforward by adding methane gas during poly-silicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

Because the device by Nakamura et al detects light that traverses the floating gate (FG) material (because the active region is located between the n+ source and drain regions) (see Figure 1) there is ample motivation to include the teaching by Halvis et al in this respect in the device by Nakamura et al. Combination of said teaching and said device is straightforward by adding methane gas during polysilicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

On claim 81: Nakamura et al teach a floating gate transistor comprising a source region and a drain region formed in a substrate, a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); a floating gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator, said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be

either floating or controlled). The floating gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

14. ***Claims 36 and 98*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (ISSN #: 0018-9383) in view of Halvis et al (5,369,040). Nakamura et al teach a floating gate transistor comprising a source region and a drain region (n+ regions in the p substrate; cf. Figure 1), a channel region in the substrate between the source region and the drain region (cf. title, abstract, and page 1693, "Introduction" (see Figure 1) and "Operation of the SFG Pixel", see Figure 1); and a (floating) gate (cf. abstract and "Introduction on page 1693) separated from the channel region by an insulator. Said source, drain, channel, and insulator also being inherent in the MOS transistor (cf. abstract) taught by Nakamura et al; and a control gate BG separated from the floating gate by an inter-gate dielectric (if the material between the gates would not be a dielectric the gates would not be electrically independent and hence both would be either floating or controlled). The (floating) gate is made of polysilicon (double-poly process used in the implementation; see Wolf (pp. 311-312) for definition of double-poly process; see page 1694 in Nakamura et al, "Image Sensor Architecture", first paragraph for double-poly process by Nakamura et al).

Nakamura et al do not necessarily teach the further limitation that the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$ with x selected to be greater

than 0.5. However, it would have been obvious to replace the floating gate material with $Si_{1-x}C_x$ with x between 0.1 and 0.5 in view of Halvis et al, who teach in the art of MOS photodetectors (cf. title and abstract), hence analogous art, that the floating gate can be made more transparent by adding up to 50% carbon, i.e., only infinitesimally less than x>0.5, to the silicon, thereby increasing the efficiency of the device (cf. abstract and col. 3, l. 32-43). The prior art range thus only infinitesimally fails to overlap with the range as claimed. Applicant's disclosure does not explain why it is critical to the invention to make x infinitesimally greater than 0.5 thus fulfilling the limitation in the claim, instead of infinitesimally less than 0.5 as taught by Halvis et al: the "Summary of the Invention" rather allows for the range $0 < x < 1$ (see pages 3-5), while other claims in the same invention cover rather complementary ranges, such as $0.1 < x < 0.5$. Furthermore, according to Applicant the value of x in one embodiment is selected to establish a desired value for the barrier energy between the gate and the underlying insulator; however, the energy gap of $Si_{1-x}C_x$, and hence said barrier energy is a continuous function of the stoichiometric parameter x (a polynomial). Therefore, said barrier energy has substantially the same value for x infinitesimally less than 0.5 and for x infinitesimally greater than 0.5. The burden is to Applicant to show otherwise, i.e., to show said infinitesimal difference in x makes a critical difference in the invention. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson,

65 USPQ2d 1379 (CA FC 2003). Because the device by Chiang et al detects light that traverses the gate material there is ample motivation to include the teaching by Halvis et al in this respect in the device by Chiang et al. Combination of said teaching and said device is straightforward by adding methane gas during poly-silicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected. Because the device by Nakamura et al detects light that traverses the floating gate (FG) material (because the active region is located between the n+ source and drain regions) (see Figure 1) there is ample motivation to include the teaching by Halvis et al in this respect in the device by Nakamura et al. Combination of said teaching and said device is straightforward by adding methane gas during polysilicon growth or using ion implantation as recommended by Halvis et al (cf. col. 3, l. 44-51). Success in implementing the combination can therefore be reasonably expected.

On claim 98: as mentioned, said gate is a floating gate (FG) (cf. Figure 1 and loc. cit.), and the device by Nakamura et al further comprises a control gate BG separated from said floating gate by an inter-gate dielectric comprising silicon dioxide.

Allowable Subject Matter

15. ***Claims 83-85*** are allowable over the prior art. The following is a statement of reasons for the indication of allowable subject matter: a floating gate transistor with source, drain, channel and gate insulator with floating gate and control gate is in the prior art (Nakamura et al, loc.cit.). However, the limitation that the floating gate material

comprises a silicon carbide compound $Si_{1-x}C_x$ wherein x is selected between 0.75 and 1.0 has not been found (the closest value for the stoichiometric parameter x found in the prior art was a limit point of 0.5). Previously cited rejection over Fujiwara (5,798,548) in view of Weitzel et al (5,661,312) and Hamakawa et al (JP357126175A) has been withdrawn: although the examiner maintains that material selection by Weitzel et al for the gate has been prompted by breakdown considerations as delineated in the previous Office Action (Paper No. 16, "Response to Arguments") (see especially col. 1, l. 58-60) the art by Hamakawa et al is insufficiently analogous to conclude obviousness: the lack of analogy stems mainly from the PIN diode rather than field effect type device taught by Hamakawa et al (see English abstract). Although carbon (Si_0C_1) gates in insulated gate field effect transistors are known (e.g., Ukai et al, 5,910,665), their inclusion together with a control gate, the carbon gate being a floating gate, has not been found to date.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JPM
May 7, 2004